

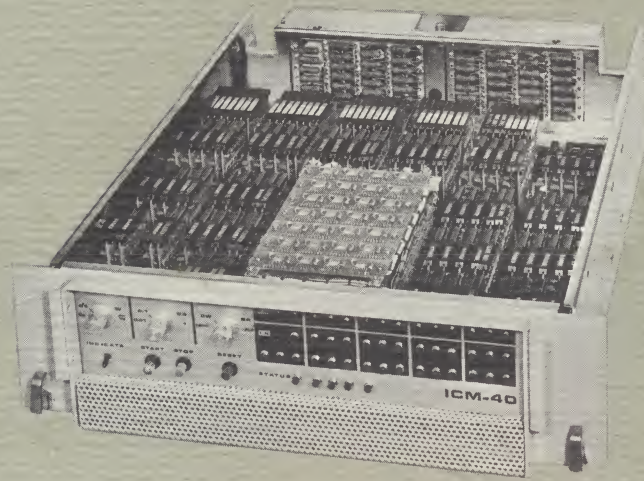


INTEGRATED CIRCUIT
MAGNETIC CORE MEMORIES SERIES ICM-40



COMPUTER CONTROL COMPANY, INC.

SERIES ICM-40
integrated circuit
magnetic core memories



standard features:

- 1 μ sec full cycle
- Monolithic integrated circuitry
- Almost $\frac{1}{4}$ million bits in one $5\frac{1}{4}$ " high module
- Temperature range 0° to 50°C
- Non-volatile start up/shut down
- Power failure sensing and protection
- Front-access slide-out or vertical swing-out packaging
- Line drivers for all outputs
- Modular construction
- Output markers: data ready, memory busy, and end of cycle
- Self-contained cooling
- Wire-wrap connections for maximum reliability
- External clear for address and data register

The ICM-40 features 1 microsecond, full cycle operation plus access time of less than 500 nanoseconds — the first standard coincident-current integrated circuit core memory to offer this speed. The memory system is basically constructed with Computer Control Company, Inc. μ -PAC monolithic integrated circuit modules, which provide almost $\frac{1}{4}$ million bits of economical high-speed storage in a single compact $5\frac{1}{4}$ " high unit. The modules, plus the application of a simplified accessing technique, result in a fast, versatile and reliable integrated circuit memory at a very low cost per bit.

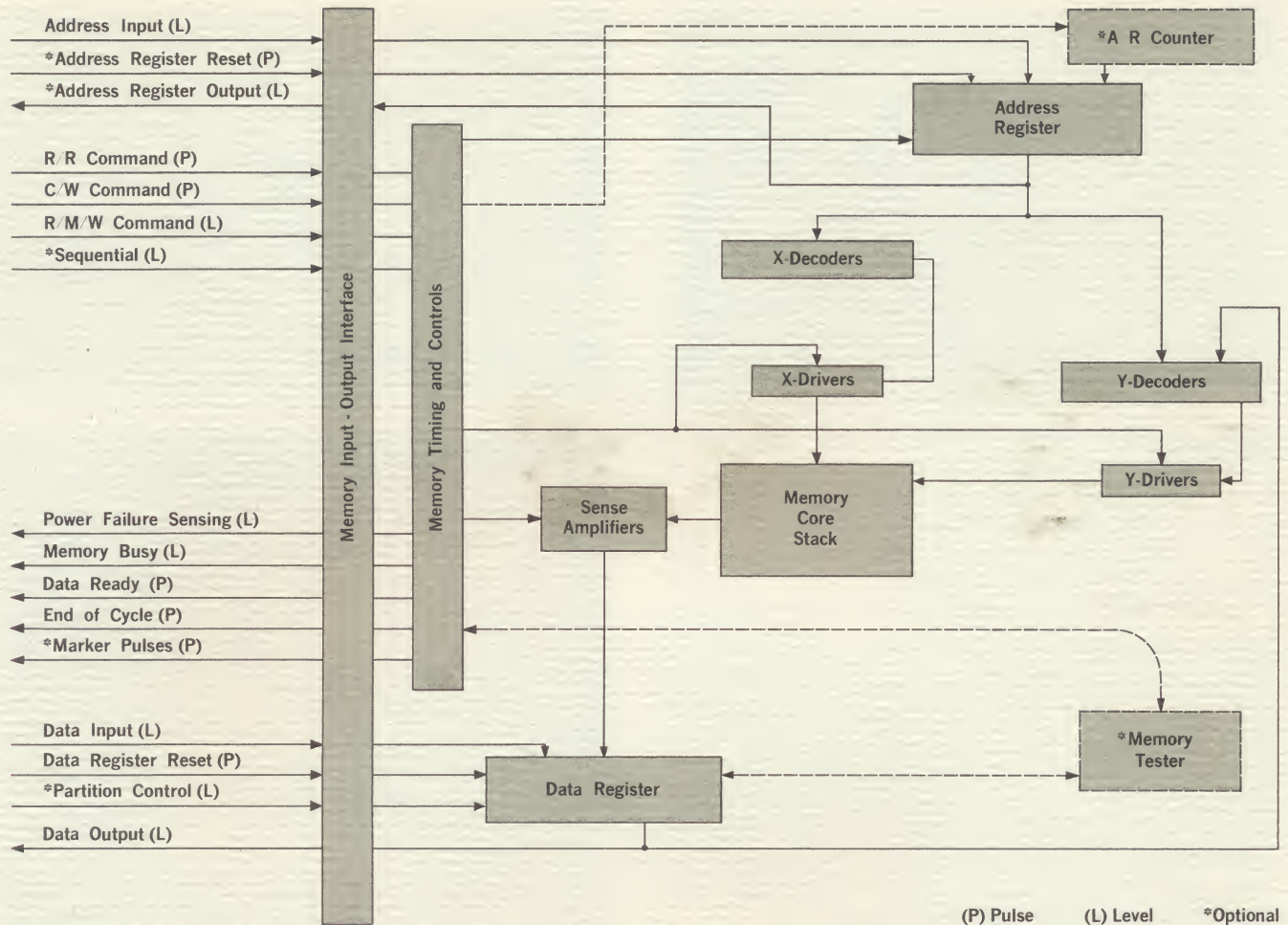
The system is based on a three-wire, coincident-current magnetic core array. All logic, addressing, decoding, control, line driving and sensing functions utilize monolithic integrated circuitry. Production techniques proven in 3C's own facility (as well as those of other major manufacturers of integrated circuits) assure the highest level of quality control and environmental stability. The only active discrete components are the core stack selection switches and delay-line drivers. These components employ conservatively derated silicon semiconductors which operate well below their maximum ratings to assure long life and high reliability.

The small size of the ICM-40 does not sacrifice ease

of maintenance. All of the circuitry is packaged on readily accessible, removable, printed-circuit μ -PAC modules. The ICM-40 system module is packaged in a $5\frac{1}{4}$ " high unit designed to mount in a standard 24" deep, 19" equipment cabinet or rack. Maintenance, when required, is simplified since each memory unit is housed in a sliding-drawer which, when pulled out, tilts in several positions. The ICM-40 is also available in a housing designed for vertical mounting which swings clear of its rack for ready access to all internal components.

The ICM-40, when used in conjunction with the MP-40 power supply, is non-volatile on start up/shut down or power failure. Thus, no loss of information will occur when power is applied or removed or when a power failure occurs. The ICM-40 is also organized so that there is no necessity to normalize the system before operation.

As standard features, each ICM-40 memory is equipped with line drivers. The receiving and driving circuitry provides the memory with line noise immunity and impedance matching for twisted pair output cables. The memory is a self-contained system which includes address and data registers, internal delay-line timing and control, sense amplifiers, selection switches, and cooling.



basic elements

Memory Timing and Control accepts and interprets the input commands and provides the sequence of pulses needed to carry out the specific operation. Timing is derived using close-tolerance passive delay lines. In addition to the internal control signals, the timing circuitry generates the memory busy, data ready, and end of cycle output signals.

Address Register transfers the incoming address from the single-ended address input lines (or from the address counter during sequential operation) upon receipt of a clear/write or read/restore command. The address register stores this information until a new address and new cycle command are received. Outputs from the address register drive the selection switch decoding matrices.

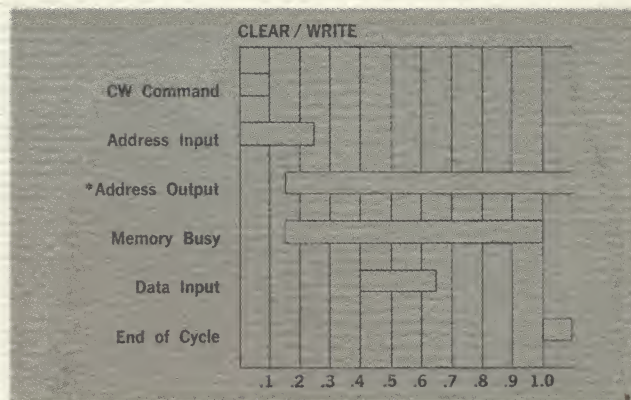
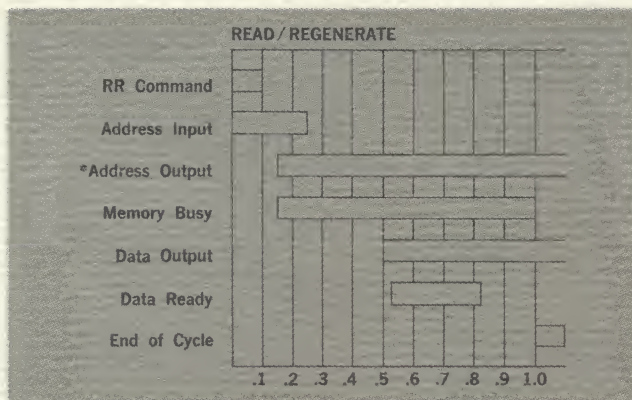
Selection of a particular address is made by simultaneous excitation of the X and Y drive lines. Information from the address register is decoded to select one X line by a matrix of read/write selection switches and one Y line by a similar switch matrix. The selected combination of X and Y read/write switches allows a particular address to be accessed for reading from or writing into the core array. Y selection switches are decoded for each bit of the data word. During the

write or restore portion of a cycle, these Y switches control the data to be stored in the core array.

Core Array consists of a number of identical core planes and the associated diode matrices and bussing. The core planes are three-wire, coincident-current planes utilizing 30 mil ferrite cores. Sense windings in the planes link all of the addresses for a particular bit. Due to the logical organization of the system, inhibit windings are not required.

Sense amplifiers receive signals from the sense windings. They are monolithic integrated circuits that provide common-mode noise rejection, controlled signal amplification, threshold and time discrimination and pulse standardization. A sense winding, common to all addresses for a particular bit in the core array, detects the output signal from the selected core.

Data Register receives incoming data from single-ended input lines during a clear/write cycle. The outputs of the register control the Y selection switches to store the data in the core array. During a read/restore cycle, the outputs of the sense amplifiers are transferred to the data register, which staticizes the output until the next command pulse.



operation

INPUT SIGNALS

All inputs to the memory terminate in diode-coupled transistor (DTL) inverters. The use of DTL inverters guarantees a high noise immunity and stability. Thus, the length of communicating lines to the memory, even in a noisy system environment, becomes a less critical factor in memory operation. The resulting noise protection of the input gates is nominally 1.2 volts. Since circuitry is DC coupled, rise and fall time specifications also become less important.

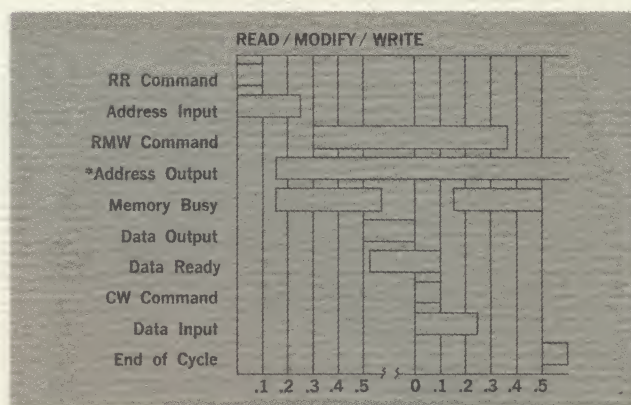
a. **Address-Register Inputs** are entered one line per bit, with a logical "ONE" input of +3.0 to +6.5 volts to set the corresponding address-register flip-flop. Address register inputs must be present and stable before the read/restore or clear/write pulse rises to 10% of its value. They must remain stable for at least 250 nanoseconds after the 90% point of the read/restore or clear/write pulse leading edge.

b. **Data-Register Input** signals must be stable no later than 400 nanoseconds after the initiation of a clear/write command. They must remain stable for the next 250 nanoseconds of the cycle.

c. **Read Regenerate Command (R/R)** is an input pulse (negative going), the leading edge of which initiates the read/restore memory cycle. This command must remain at 0 volts for at least 100 nanoseconds.

d. **Clear/Write Command (C/W)** is an input pulse (negative going), the leading edge of which initiates a clear/write memory cycle. This command must remain at 0 volts for at least 100 nanoseconds.

e. **Read/Modify/Write Command (R/M/W)** is an input level which, when asserted within 300 nanoseconds after a read/restore command, causes the cycle to terminate following data read-out. If this level is maintained and a subsequent clear/write pulse is furnished, the memory will write into the



*STANDARD OPTION

address previously read, data provided on the information input lines, thus completing the read/modify/write operation.

OUTPUT SIGNALS

All output signals from the memory are transmitted via cable drivers equipped with a unique short-circuit-protection network to prevent circuit damage due to accidental grounding of the output. These cable drivers are series terminated at the source to match twisted pair characteristic impedances between 50 and 100 ohms. They are capable of driving up to 10 feet of twisted pair cable. Loading at the receiving end should exceed 1000 ohms for reliable operation.

a. **Data Outputs** from the information register flip-flops are wired to cable-driver circuits. Data access time is equal to or less than 0.5 microseconds.

b. **Memory Busy** signal level rises 150 nanoseconds after the initiation of either a read/restore or clear/write and remains static until the end of cycle signal is generated.

c. **Data Ready** output signal indicates when information is available at the output interface and has a minimum duration of 300 nanoseconds. The signal is generated immediately after the transition of the information register output.

d. **End of Cycle** signal has a duration of 300 nanoseconds and reaches its final value immediately after the completion of the memory cycle.

specifications

Memory Capacity: 4,096 words 4-28 bits
8,192 words 4-28 bits
16,384 words 4-14 bits
Multiple module capability allows the ICM-40 to be expanded to larger word size or capacity.

Operating speed: 1.0 microsecond for C/W and R/R
1.25 microseconds for R/M/W

Access time: <0.5 microseconds

Logic levels (Input):

ZERO 0.0 volts to +1.0 volts
ONE +3.0 to +6.5 volts

Logic levels (Output):

ZERO 0.0 volts to +0.40 volts
ONE +4.0 volts to +6.5 volts

Output drive capability:

10 feet of twisted pair cable

Power: 115 or 230 volts ($\pm 15\%$)
50 or 60 cps (± 1 cps)

Physical characteristics:

Height: 5 $\frac{1}{4}$ "
Width: 19"
Depth: 22"
Weight: <45 lbs.

Environment:

Operating temp 0° to 50°C

Non-operating temp -25°C to +80°C

Humidity 95% without condensation

Shock and vibration normal shipping conditions

1. **Sequential Addressing** is provided by the addition of a separate counter which supplies the address register with a sequenced address on command. The address is provided to the address register at the beginning of each sequential operation. The counter is incremented to the next address while the memory is performing the operating cycle.

2. **Memory Clear** provides a means of clearing all memory locations by asserting the sequential control line, the read/restore line and the read/modify/write line. All three levels must be held asserted for a period determined by the number of words stored in the memory. This option is provided in all memories equipped with the sequential address register option.

3. **Partitioning** allows the data register to be divided into two, three, or four independently controllable groups. This permits a selected portion of the data word to be changed without altering or destroying the rest of the word. Cycle time is not extended during this operation. Partitioning control levels must be stable no later than 50 nanoseconds after the initiation of a cycle command and must remain stable until 950 nanoseconds.

4. **Memory Tester** unit which is built into the ICM-40 is offered as a standard option. The tester includes a pattern generator capable of producing four fixed patterns, which are selected by a front-panel switch. These patterns include all "ONES", all "ZEROS", worst-case pattern, and worst-pattern complement. The tester loads the selected pattern into the memory and checks this pattern for accuracy during unload. If an error should occur, the test cycle will be interrupted and will indicate the address of the error and the data register bit that is in error. If desired, the tester controls may be set to allow test cycles to be continued in the presence of an error.

5. **Indicators** are individual display lamps for each of the address register and data register flip-flops. Other control flip-flops may be displayed to indicate the operating mode or condition of the memory.

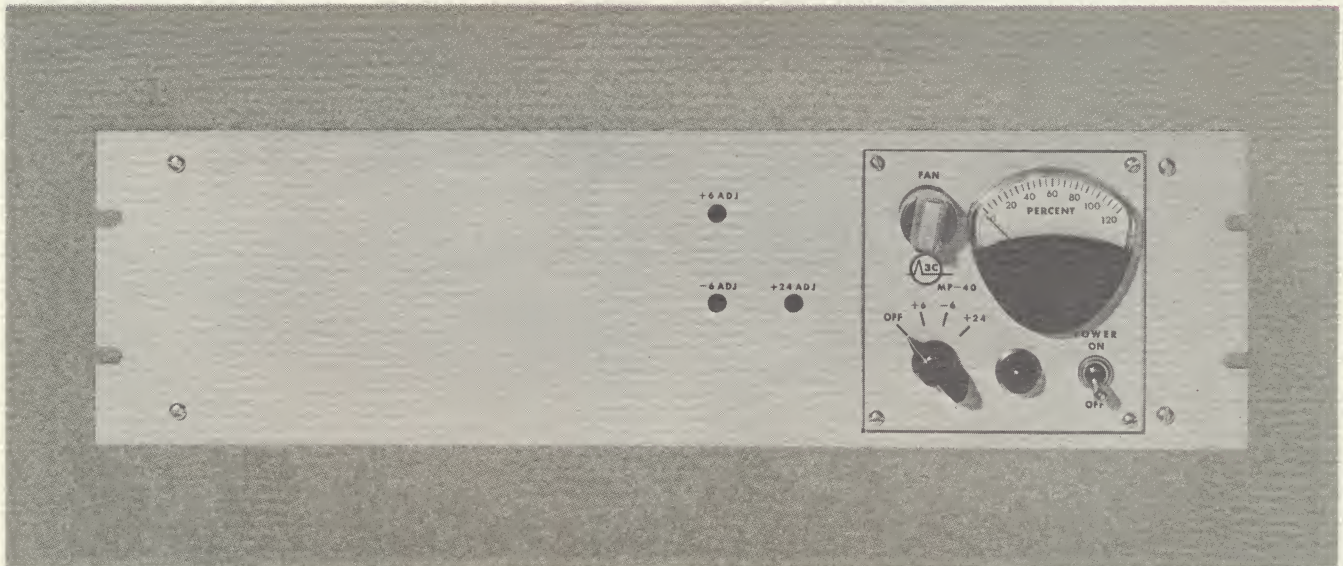
6. **Address Register Outputs** are single-ended levels which reach their significant transitions approximately 200 nanoseconds after either the R/R or C/W signals.

7. **Marker Pulses** (1 to 4) can be made available at specified times during memory cycles.

8. **Address Register Reset** is an input pulse (minimum width 100 nsec.). Assertion of this pulse resets the address counter which supplies the address register when operating in a sequential mode.

9. **Data Register Reset** is an input pulse. When the pulse is applied, it resets the data register.

power supply model MP-40



The Model MP-40 power supply is a separate rack-mountable unit which has a panel height of 5¼". The supply provides sufficient power for 28-bit ICM-40 memories of capacities up to 16,384 words. The supply has built-in power-failure sensing and protection. This provision assures no loss of information in the memory due to power turn-on, turn-off or failure. If desired, an optional voltmeter may be installed on the supply front panel. The MP-40 supply utilizes all-silicon semiconductors and features overload, line-transient, over-voltage, and thermal protection. It also has a temperature-compensated drive voltage.

This supply is available in two models:

1. Model MP-40, which operates from input power of 115 or 230 volts AC ($\pm 15\%$) at 60 cps.
2. Model MP-40E, which is designed to accept an input voltage of 115 or 230 volts AC ($\pm 15\%$) at 50 cps.

Environmental operating temperature range is 0°C to +60°C with a storage temperature of -25°C to +80°C.

Overall dimensions: Height — 5¼"
 Width — 19"
 Depth — 17¼"

Weight: 60 lbs.

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3C warranty

a) Computer Control Company, Inc. warrants all 3C instrument products against defects in workmanship, materials and construction under normal use and service for a period of ONE YEAR from the date of shipment, except that liability for semiconductors, switches, and potentiometers shall conform and be limited to the obligation of the original manufacturers' warranties covering these components.

b) This warranty does not extend to any of our products which have been subjected to misuse, neglect, accident, or improper installation or application. Nor shall it extend to products which have been repaired or altered outside of our factory.

c) For service under this warranty, please advise the factory promptly of all pertinent details. Transportation charges covering return of defective products to our factory shall be at our expense if such products are determined to be defective within the limitations of this warranty. Computer Control Company, Inc. will repair or replace the defective product in accordance with its own best judgment.

d) Computer Control Company, Inc. requests immediate notification of any claims arising from damage in transit in order to determine if carrier responsibility exists.

other 3C products and services

A major area of 3C specialization is the design, development and manufacture of general purpose digital computers and special purpose systems.

3C is also a leading supplier of digital logic modules, pulse current generators and digital program generators.



COMPUTER CONTROL COMPANY, INC.

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